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TYNEMOUTH SOFTWARE Z80 CPU, CLOCK AND RESET FOR RC2014

PARTS LIST

CAPACITORS – CERAMIC RATED 6.3V OR HIGHER

2 x 22pF 0.1" spacing *(usually marked 22p or 220) – check crystal, some require different values, e.g. 18pF*
1 x 10nF axial *(usually marked 10n or 103)*
4 x 100nF axial *(usually marked 100n or 104)*
1 x 1uF axial *(usually marked 1u or 105)*

RESISTORS – ALL ¼W 5% OR BETTER (4 BAND RESISTOR COLOUR CODES SHOWN)

3 x 1KΩ
5 x 10KΩ
3 x 1MΩ

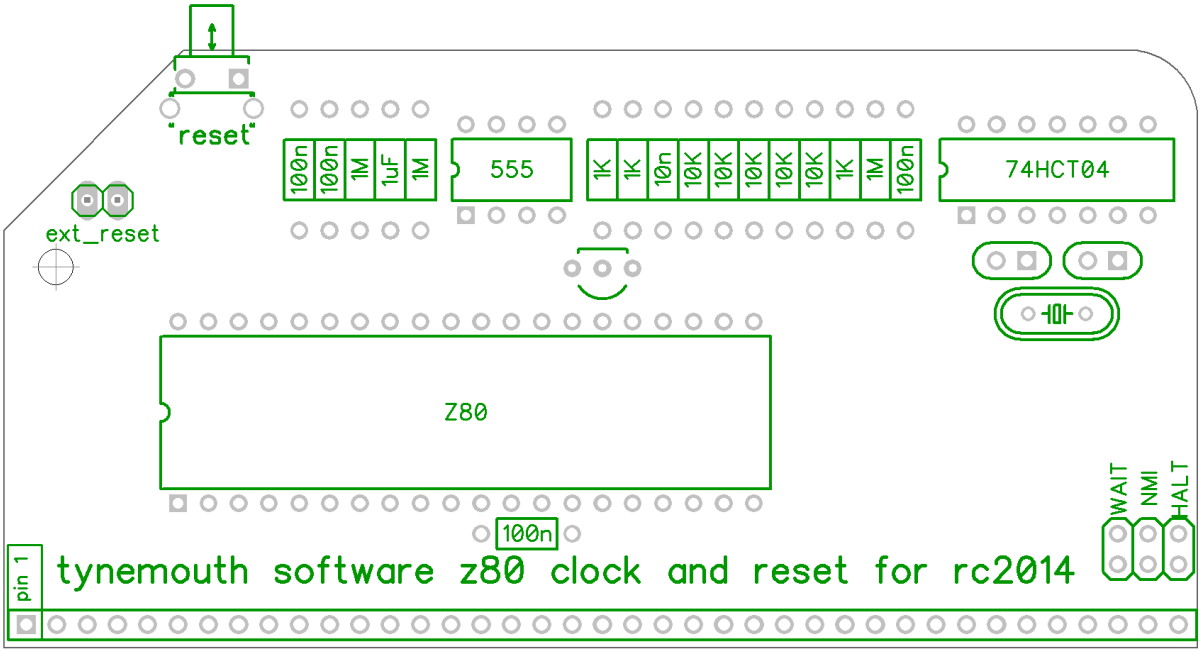
SEMICONDUCTORS

1 x BC548B or similar NPN transistor
1 x 74HCT04
1 x 555 timer / NE555P / LM555 / 7555 etc.
1 x Z80 CPU / NEC D780 / Zilog Z84C0008PEG / Z84C0010PEG (*8MHz or higher rated*)
1 x HC49U Crystal – 7.3728 MHz (*or as required*).

CONNECTORS / SWITCHES

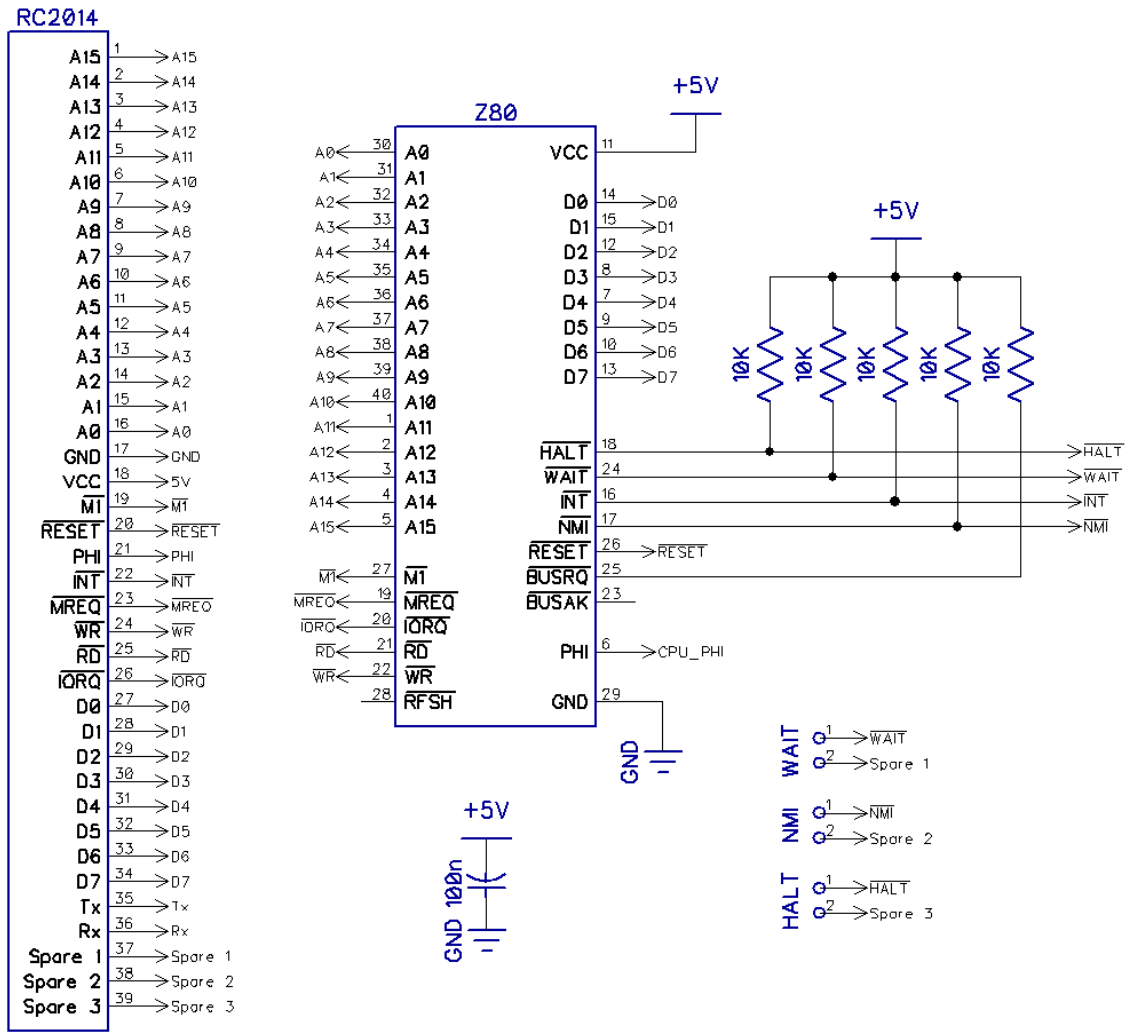
1 x 39 way 0.1" right angled header (buy 40 way and snap off 1pin)
Optional 3x 0.1" 2 way header and jumpers if using extended signals
Optional 1x 0.1" 2 way header for external reset switch
Optional right angled tactile switch for reset

COMPONENT PLACEMENT



Z80 CPU

RC2014 CONNECTOR AND CPU SCHEMATIC



CONNECTIONS

The input signals to the Z80 microprocessor are pulled high by the 10KΩ resistors.

INT is connected to the RC2014 bus

HALT, WAIT and NMI are not normally part of the RC2014 bus, and jumpers are provided to connect these to the three spare pins, for future use.

BUSRQ is pulled high, but is otherwise unconnected.

BUSAK is not connected.

The output signals (M1, MREQ, IORQ, RD, WR) are connected to the bus

RFSH is not connected

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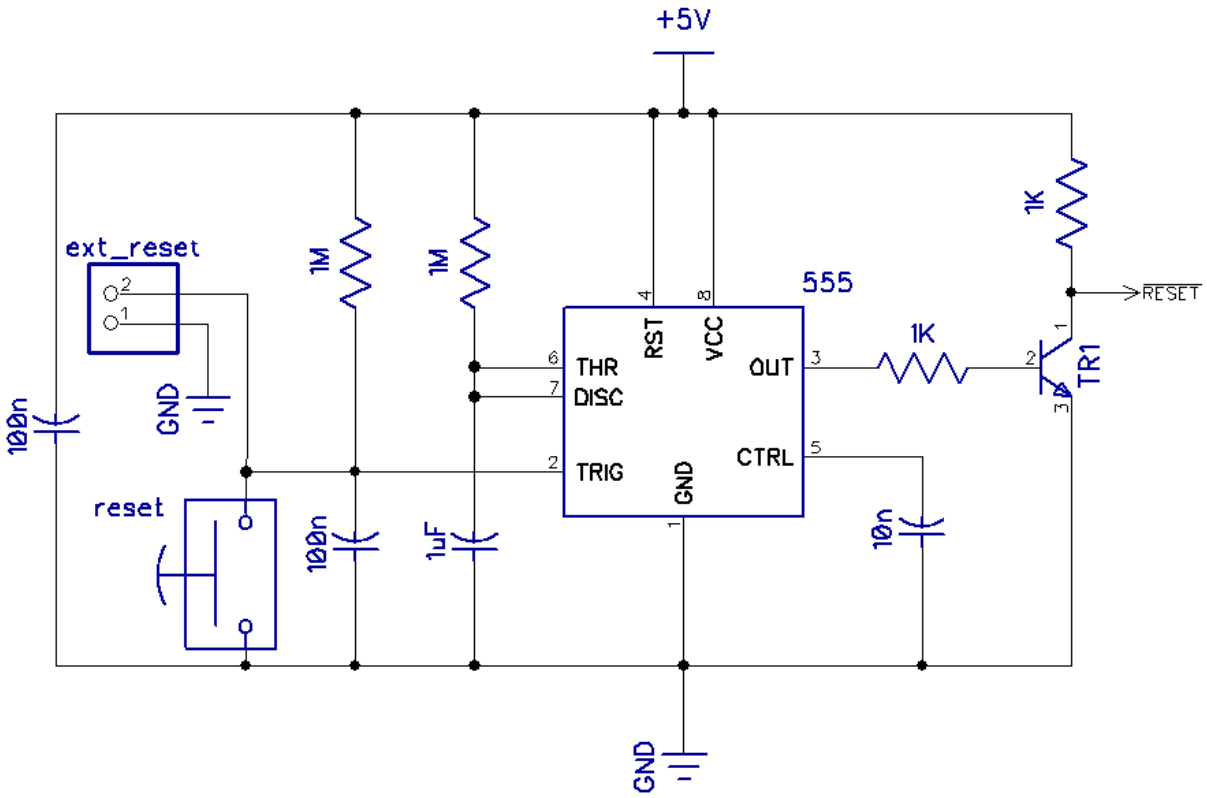
RESET CIRCUIT

SCHEMATIC



OVERVIEW

This reset circuit is similar to that used in many 1980s home computers. The 555 timer is used to generate a clean reset pulse at power up and when the reset switch is pressed.

The reset pulse timing is set by the 1µF capacitor and 1MΩ resistor connected to pins 6 and 7. The time is calculated as

1.1 x R x C

With those values, the reset pulse will be 1.1 seconds long. The values can be changed if you wish to alter the length of the reset pulse.

The 100nF capacitor and 1MΩ resistor will provide a brief pulse to the trigger input on pin 2 to start the 1.1 second timer. This will happen at power on and when the reset switch is pressed.

In normal operation, the reset line is pulled high by the 1KΩ resistor. When the reset pulse is active, the transistor pulls the line low. This arrangement is used to allow other devices on the bus, and the backplane itself to pull the reset line low. It is recommended to use the reset switch on this board or fit an external reset switch to the 2 pin header, as this will trigger the 555 to generate a clean reset pulse.

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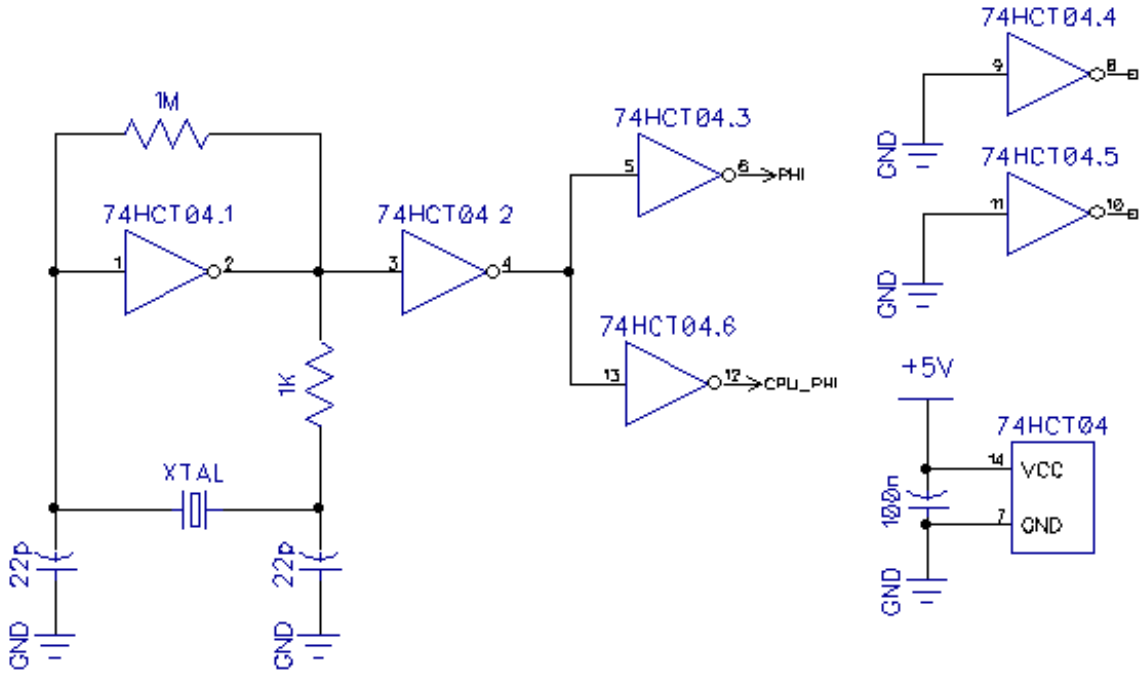
CLOCK CIRCUIT

SCHEMATIC



OVERVIEW

This is a fairly standard crystal oscillator circuit based around an inverter gate. The clock signal is buffered by the second gate.

This buffered signal is then fed to two separate buffers, one which drives the CPU with it's own clean clock signal, the other provides the clock signal to the RC2014 bus. This additional buffering is not really necessary, but the gates are otherwise unused.

A 7.3728MHz crystal would typically be used as this value can be used by the RC2014 comms boards to divide down to generate standard baud rates. A 3.6864Mhz crystal will also divide down to BAUD rate levels, but at half speed (e.g. 115,200 settings will give 57,600 etc.)

If you are not using the system clock for RS232, other value crystals can be used depending on the application.

The capacitor values shown will vary depending on the crystal used. The value is usually stated in the datasheet as load capacitance, and will be around 18-22pF.

The two spare inputs are tied low and the gate outputs are unused.